ABSTRACT OF THE DISCLOSURE

System, methods, and apparatus for verifying microcircuit designs by interleaving

between random and formal simulation techniques to identify input traces useful for

driving DUTs into sequences of device states. In a method aspect the invention provides

5   process for beginning random simulation of a sequence of states of a microcircuit design

by inputting a sequence of random input vectors to a DUT model in order to obtain a

sequence of random simulation states; monitoring a simulation coverage progress metric

to determine a preference for switching from random simulation to formal methods of

simulating states in the DUT; beginning formal simulation of states in the DUT and

10   monitoring a formal coverage progress metric to determine a preference for resuming

random simulation of states of said microcircuit design; and resuming random simulation.

Preferably the process of interleaving simulation methods continues until an input vector

suitable for driving the DUT model into each of a set of previously-identified goal states

has been obtained.

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